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Amendments to the Claims

1. (Currently Amended) A memory cell comprising:

- a semiconductor substrate;
- a P well formed in said semiconductor substrate;
- an N well formed in said semiconductor substrate adjacent to said P well;
- an N type active region defined in said P well;
- a P type active region defined in said N well;
- an isolation region arranged to isolate said N type active region from said P type active region;
- a polysilicide gate electrode structure composed of a polycrystalline silicon film and an overlying metal, metal silicide, or metal nitride film, wherein said polycrystalline silicon film comprises an N+ polysilicon layer over said N type active region and a P+ polysilicon layer over said P type active region; and
- an oxide diffusion barrier layer formed in said polysilicide gate electrode structure over on a portion of said polycrystalline silicon film between said polycrystalline silicon film and said metal, metal silicide, or metal nitride film, and over only a portion of said isolation region.

2. (Currently Amended) A memory cell comprising:

- a semiconductor substrate;
- a P well formed in said semiconductor substrate;
- an N well formed in said semiconductor substrate;
- an NMOS transistor defining an N type active region in said P well;
- a PMOS transistor defining a P type active region in said N well;
- an isolation region arranged to isolate said N type active region from said P type active region;
- a polysilicide gate electrode structure composed of a polycrystalline silicon film and an overlying metal, metal silicide, or metal nitride film, wherein said polycrystalline silicon film comprises an N+ polysilicon layer forming a portion of said NMOS transistor, and a P+ polysilicon layer forming a portion of said PMOS transistor; and

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an oxide diffusion barrier layer formed in said polysilicide gate electrode structure overon a portion of said polycrystalline silicon film between said polycrystalline silicon film and said metal, metal silicide, or metal nitride film, and over only a portion of said isolation region.

3. (Currently Amended) A memory cell comprising:

a semiconductor substrate having first and second gate oxide layers;
a P well formed in said semiconductor substrate;
an N well formed in said semiconductor substrate;
an NMOS transistor defining an N type active region in said P well;
a PMOS transistor defining a P type active region in said N well;
an isolation region arranged to isolate said N type active region from said P type active region, and separate said first and second gate oxide layers;

a polysilicide gate electrode structure composed of a polycrystalline silicon film and an overlying metal, metal silicide, or metal nitride film, wherein said polycrystalline silicon film comprises an N+ polysilicon layer on said first gate oxide layer and on a first portion of said isolation region and forming a portion of said NMOS transistor, and a P+ polysilicon layer on said second gate oxide layer and on a second portion of said isolation region and forming a portion of said PMOS transistor; and

an oxide diffusion barrier layer formed in said polysilicide gate electrode structure between said polycrystalline silicon film and said metal, metal silicide, or metal nitride film and over only one of said first and second portions of said isolation region, wherein said polysilicide gate electrode structure and said oxide diffusion barrier layer are arranged such that migration of P+ dopants from said P+ polysilicon layer to said overlying metal, metal silicide, or metal nitride film is significantly impeded by said oxide diffusion barrier layer.

4. (Currently Amended) A memory cell comprising:

a semiconductor substrate;
a P well formed in said semiconductor substrate;

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an N well formed in said semiconductor substrate;
an NMOS transistor defining an N type active region in said P well;
a PMOS transistor defining a P type active region in said N well;
an isolation region arranged to isolate said N type active region from said P type active region;

a polysilicide gate electrode structure composed of a polycrystalline silicon film and an overlying metal, metal silicide, or metal nitride film, wherein said polycrystalline silicon film comprises an N+ polysilicon layer forming a portion of said NMOS transistor and a P+ polysilicon layer forming a portion of said PMOS transistor; and

an oxide diffusion barrier layer formed in said polysilicide gate electrode structure ~~over on a portion of~~ said P+ polysilicon layer between said P+ polysilicon layer and said metal, metal silicide, or metal nitride film and over only a portion of said isolation region, wherein said oxide diffusion barrier layer does not extend over a portion of said N+ polysilicon layer.

5. (Currently Amended) A memory cell comprising:

a semiconductor substrate;
a P well formed in said semiconductor substrate;
an N well formed in said semiconductor substrate;
an NMOS transistor defining an N type active region in said P well;
a PMOS transistor defining a P type active region in said N well;
an isolation region arranged to isolate said N type active region from said P type active region;

a polysilicide gate electrode structure composed of a polycrystalline silicon film and an overlying metal, metal silicide, or metal nitride film, wherein said polycrystalline silicon film comprises an N+ polysilicon layer forming a portion of said NMOS transistor and a P+ polysilicon layer forming a portion of said PMOS transistor; and

an oxide diffusion barrier layer formed in said polysilicide gate electrode structure ~~over on~~ said P+ polysilicon layer between said P+ polysilicon layer and said metal, metal silicide, or metal nitride film and over only a portion of said isolation region, wherein

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said oxide diffusion barrier layer is arranged such that said metal, metal silicide, or metal nitride film defines an N type common boundary with said N+ polysilicon layer that is significantly larger than a P type common boundary defined by said metal, metal silicide, or metal nitride film and said P+ polysilicon layer.

6. (Currently Amended) A memory cell comprising:

- a semiconductor substrate;
- a P well formed in said semiconductor substrate;
- an N well formed in said semiconductor substrate;
- an NMOS transistor defining an N type active region in said P well;
- a PMOS transistor defining a P type active region in said N well;
- an isolation region arranged to isolate said N type active region from said P type active region;
- a polysilicide gate electrode structure composed of a polycrystalline silicon film and an overlying metal, metal silicide, or metal nitride film, wherein said polycrystalline silicon film comprises an N+ polysilicon layer forming a portion of said NMOS transistor and a P+ polysilicon layer forming a portion of said PMOS transistor; and
- an oxide diffusion barrier layer formed in said polysilicide gate electrode structure between said polycrystalline silicon film and said metal, metal silicide, or metal nitride film and over only a portion of said isolation region, wherein said polysilicide gate electrode structure and said oxide diffusion barrier layer are arranged such that migration of N+ dopants from said N+ polysilicon layer to said overlying metal, metal silicide, or metal nitride film is significantly impeded by said oxide diffusion barrier layer.

7. (Currently Amended) A memory cell comprising:

- a semiconductor substrate;
- a P well formed in said semiconductor substrate;
- an N well formed in said semiconductor substrate;
- an NMOS transistor defining an N type active region in said P well;
- a PMOS transistor defining a P type active region in said N well;

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an isolation region arranged to isolate said N type active region from said P type active region;

a polysilicide gate electrode structure composed of a polycrystalline silicon film and an overlying metal, metal silicide, or metal nitride film, wherein said polycrystalline silicon film comprises an N+ polysilicon layer forming a portion of said NMOS transistor and a P+ polysilicon layer forming a portion of said PMOS transistor; and

an oxide diffusion barrier layer formed in said polysilicide gate electrode structure over a portion of said N+ polysilicon layer between said N+ polysilicon layer and said metal, metal silicide, or metal nitride film and over only a portion of said isolation region, wherein said oxide diffusion barrier layer does not extend over a portion of said P+ polysilicon layer.

8. (Currently Amended) A memory cell comprising:

a semiconductor substrate;

a P well formed in said semiconductor substrate;

an N well formed in said semiconductor substrate;

an NMOS transistor defining an N type active region in said P well;

a PMOS transistor defining a P type active region in said N well;

an isolation region arranged to isolate said N type active region from said P type active region;

a polysilicide gate electrode structure composed of a polycrystalline silicon film and an overlying metal, metal silicide, or metal nitride film, wherein said polycrystalline silicon film comprises an N+ polysilicon layer forming a portion of said NMOS transistor and a P+ polysilicon layer forming a portion of said PMOS transistor; and

an oxide diffusion barrier layer formed in said polysilicide gate electrode structure over a portion of said N+ polysilicon layer between said N+ polysilicon layer and said metal, metal silicide, or metal nitride film and over only a portion of said isolation region, wherein said oxide diffusion barrier layer is arranged such that said metal, metal silicide, or metal nitride film defines a P type common boundary with said P+ polysilicon layer

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that is significantly larger than an N type common boundary defined by said metal, metal silicide, or metal nitride film and said N+ polysilicon layer.

9. (Cancel) A memory cell comprising:

- ~~—— a semiconductor substrate;~~
- ~~—— a P well formed in said semiconductor substrate;~~
- ~~—— an N well formed in said semiconductor substrate;~~
- ~~—— an NMOS transistor defining an N type active region in said P well;~~
- ~~—— a PMOS transistor defining a P type active region in said N well;~~
- ~~—— an isolation region arranged to isolate said N type active region from said P type active region;~~
- ~~—— a polysilicide gate electrode structure composed of a polycrystalline silicon film and an overlying metal, metal silicide, or metal nitride film, wherein said polycrystalline silicon film comprises an N+ polysilicon layer forming a portion of said NMOS transistor and a P+ polysilicon layer forming a portion of said PMOS transistor; and~~
- ~~—— an oxide diffusion barrier layer formed in said polysilicide gate electrode structure over said N+ polysilicon layer and said P+ polysilicon layer between said polycrystalline silicon film and said metal, metal silicide, or metal nitride film, wherein said polysilicide gate electrode structure and said oxide diffusion barrier layer are arranged such that~~
 - ~~—— migration of P+ dopants from said P+ polysilicon layer to said overlying metal, metal silicide, or metal nitride film is significantly impeded by said oxide diffusion barrier layer and~~
 - ~~—— migration of N+ dopants from said N+ polysilicon layer to said overlying metal, metal silicide, or metal nitride film is significantly impeded by said oxide diffusion barrier layer.~~

10. (Currently Amended) An SRAM memory cell comprising:

- a semiconductor substrate;
- a P well formed in said semiconductor substrate;
- an N well formed in said semiconductor substrate;

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a flip-flop formed by two access transistors and a pair of cross coupled inverters, wherein each pair of cross-coupled inverters includes a pull up transistor and a pull down transistor, and wherein said pull-up transistor defines a P type active region in said N well and said pull-down transistor defines an N type active region in said P well;

an isolation region arranged to isolate said N type active region from said P type active region;

a polysilicide gate electrode structure composed of a polycrystalline silicon film and an overlying metal, metal silicide, or metal nitride film, wherein said polycrystalline silicon film comprises an N+ polysilicon layer forming a portion of said pull-down transistor and a P+ polysilicon layer forming a portion of said pull-up transistor; and

an oxide diffusion barrier layer formed in said polysilicide gate electrode structure between said polycrystalline silicon film and said metal, metal silicide, or metal nitride film ~~over~~ on a portion of said polycrystalline silicon film, and over only a portion of said isolation region.

11. (Currently Amended) An SRAM memory cell comprising:

a semiconductor substrate;

a P well formed in said semiconductor substrate;

an N well formed in said semiconductor substrate;

a flip-flop formed by two access transistors and a pair of cross coupled inverters, wherein each pair of cross-coupled inverters includes a pull up transistor and a pull down transistor, and wherein said pull-up transistor defines a P type active region in said N well and said pull-down transistor defines an N type active region in said P well;

an isolation region arranged to isolate said N type active region from said P type active region;

a polysilicide gate electrode structure composed of a polycrystalline silicon film having a thickness of between about 500 Å and about 4000 Å and an overlying metal, metal silicide, or metal nitride film having a thickness of between about 500 Å and 4000 Å, wherein said polycrystalline silicon film comprises an N+ polysilicon layer

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forming a portion of said pull-down transistor and a P+ polysilicon layer forming a portion of said pull-up transistor; and

an oxide diffusion barrier layer having a thickness of between about 3 Å and about 25 Å formed in said polysilicide gate electrode structure between said polycrystalline silicon film and said metal, metal silicide, or metal nitride film ~~over on~~ a portion of said polycrystalline silicon film, and over only a portion of said isolation region.

12. (Cancel) ~~An SRAM memory cell comprising:~~

- ~~—— a semiconductor substrate;~~
- ~~—— a P well formed in said semiconductor substrate;~~
- ~~—— an N well formed in said semiconductor substrate;~~
- ~~—— a flip flop formed by two access transistors and a pair of cross coupled inverters, wherein each pair of cross coupled inverters includes a pull up transistor and a pull down transistor, and wherein said pull up transistor defines a P type active region in said N well and said pull down transistor defines an N type active region in said P well;~~
- ~~—— an isolation region arranged to isolate said N type active region from said P type active region;~~
- ~~—— a polysilicide gate electrode structure composed of a polycrystalline silicon film and an overlying metal, metal silicide, or metal nitride film, wherein said polycrystalline silicon film comprises an N+ polysilicon layer forming a portion of said pull down transistor and a P+ polysilicon layer forming a portion of said pull up transistor; and~~
- ~~—— an oxide diffusion barrier layer formed in said polysilicide gate electrode structure between said polycrystalline silicon film and said metal, metal silicide, or metal nitride film over a portion of said N+ polysilicon layer and said P+ polysilicon layer.~~

13. (Currently Amended) An SRAM memory cell comprising:

- a semiconductor substrate;
- a P well formed in said semiconductor substrate;
- an N well formed in said semiconductor substrate;

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a flip-flop formed by two access transistors and a pair of cross coupled inverters, wherein each pair of cross-coupled inverters includes a pull up transistor and a pull down transistor, and wherein said pull-up transistor defines a P type active region in said N well and said pull-down transistor defines an N type active region in said P well;

an isolation region arranged to isolate said N type active region from said P type active region;

a polysilicide gate electrode structure composed of a polycrystalline silicon film and an overlying metal, metal silicide, or metal nitride film, wherein said polycrystalline silicon film comprises an N+ polysilicon layer forming a portion of said pull-down transistor and a P+ polysilicon layer forming a portion of said pull-up transistor; and

an oxide diffusion barrier layer formed in said polysilicide gate electrode structure between said polycrystalline silicon film and said metal, metal silicide, or metal nitride film and over only a portion of said isolation region, wherein said polysilicide gate electrode structure and said oxide diffusion barrier layer are arranged such that migration of P+ dopants from said P+ polysilicon layer to said overlying metal, metal silicide, or metal nitride film is significantly impeded by said oxide diffusion barrier layer.

14. (Currently Amended) An SRAM memory cell comprising:

a semiconductor substrate;

a P well formed in said semiconductor substrate;

an N well formed in said semiconductor substrate;

a flip-flop formed by two access transistors and a pair of cross coupled inverters, wherein each pair of cross-coupled inverters includes a pull up transistor and a pull down transistor, and wherein said pull-up transistor defines a P type active region in said N well and said pull-down transistor defines an N type active region in said P well;

an isolation region arranged to isolate said N type active region from said P type active region;

a polysilicide gate electrode structure composed of a polycrystalline silicon film and an overlying metal, metal silicide, or metal nitride film, wherein said polycrystalline

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silicon film comprises an N+ polysilicon layer forming a portion of said pull-down transistor and a P+ polysilicon layer forming a portion of said pull-up transistor; and
an oxide diffusion barrier layer formed in said polysilicide gate electrode structure between said polycrystalline silicon film and said metal, metal silicide, or metal nitride film and over only a portion of said isolation region, wherein said polysilicide gate electrode structure and said oxide diffusion barrier layer are arranged such that migration of N+ dopants from said N+ polysilicon layer to said overlying metal, metal silicide, or metal nitride film is significantly impeded by said oxide diffusion barrier layer.

15. (Currently Amended) A memory cell array comprising a plurality of SRAM cells arranged in rows and columns, wherein each cell of said array is connected to a word line and to a pair of bit lines and comprises:

- a semiconductor substrate;
- a P well formed in said semiconductor substrate;
- an N well formed in said semiconductor substrate;
- a flip-flop formed by two access transistors and a pair of cross coupled inverters, wherein each pair of cross-coupled inverters includes a pull up transistor and a pull down transistor, and wherein said pull-up transistor defines a P type active region in said N well and said pull-down transistor defines an N type active region in said P well;
- an isolation region arranged to isolate said N type active region from said P type active region;
- a polysilicide gate electrode structure composed of a polycrystalline silicon film and an overlying metal, metal silicide, or metal nitride film, wherein said polycrystalline silicon film comprises an N+ polysilicon layer forming a portion of said pull-down transistor and a P+ polysilicon layer forming a portion of said pull-up transistor; and
- an oxide diffusion barrier layer formed in said polysilicide gate electrode structure between said polycrystalline silicon film and said metal, metal silicide, or metal nitride film overon a portion of said polycrystalline silicon film, and over only a portion of said isolation region.

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16. (Currently Amended) A computer system including a microprocessor in communication with a memory cell array via a data communication path, wherein said memory cell array comprises a plurality of SRAM cells arranged in rows and columns, and wherein each cell of said array is connected to a word line and to a pair of bit lines and comprises:

a semiconductor substrate;

a P well formed in said semiconductor substrate;

an N well formed in said semiconductor substrate;

a flip-flop formed by two access transistors and a pair of cross coupled inverters, wherein each pair of cross-coupled inverters includes a pull up transistor and a pull down transistor, and wherein said pull-up transistor defines a P type active region in said N well and said pull-down transistor defines an N type active region in said P well;

an isolation region arranged to isolate said N type active region from said P type active region;

a polysilicide gate electrode structure composed of a polycrystalline silicon film and an overlying metal, metal silicide, or metal nitride film, wherein said polycrystalline silicon film comprises an N+ polysilicon layer forming a portion of said pull-down transistor and a P+ polysilicon layer forming a portion of said pull-up transistor; and

an oxide diffusion barrier layer formed in said polysilicide gate electrode structure between said polycrystalline silicon film and said metal, metal silicide, or metal nitride film ~~over on~~ a portion of said polycrystalline silicon film and over only a portion of said isolation region.

21. (Previously Amended) A memory cell as claimed in claim 1 wherein said oxide diffusion barrier layer comprises silicon dioxide.

22. (Previously Amended) A memory cell as claimed in claim 1 wherein said oxide diffusion barrier layer has a thickness of less than 125 Å.

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23. (Previously Amended) A memory cell as claimed in claim 1 wherein said oxide diffusion barrier layer has a thickness of between about 10 Å and about 15 Å.
24. (Previously Amended) A memory cell as claimed in claim 1 wherein said oxide diffusion barrier layer has a thickness of between about 3 Å and about 125 Å.
25. (Previously Amended) A memory cell as claimed in claim 1 wherein said oxide diffusion barrier layer has a thickness of between about 3 Å and about 50 Å.
26. (Previously Amended) A memory cell as claimed in claim 1 wherein said oxide diffusion barrier layer has a thickness of between about 3 Å and about 125 Å and said polycrystalline silicon film has a thickness of between about 500 Å and about 4000 Å.
27. (Previously Amended) A memory cell as claimed in claim 5 wherein metal, metal silicide, or metal nitride film form defines an overcoated portion of said P+ polysilicon layer and wherein said oxide diffusion barrier layer is formed in said polysilicide gate electrode structure between said metal, metal silicide, or metal nitride film and said P+ polysilicon layer over the entire extent of said overcoated portion of said P+ polysilicon layer.
28. (Previously Amended) A memory cell as claimed in claim 8 wherein metal, metal silicide, or metal nitride film form defines an overcoated portion of said N+ polysilicon layer and wherein said oxide diffusion barrier layer is formed in said polysilicide gate electrode structure between said metal, metal silicide, or metal nitride film and said N+ polysilicon layer over the entire extent of said overcoated portion of said N+ polysilicon layer.
31. (Currently Amended) A gate electrode structure for a semiconductive device having N type and P type active regions separated by an isolation region, said gate electrode structure comprising:

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a film having an N⁺ polysilicon layer over the N type active region and a P⁺ polysilicon layer over the P type active region;

an oxide layer formed ~~overon~~ a portion of said film and over only a portion of said isolation region; and

a metal, metal silicide, or metal nitride film overlaying said film and said oxide layer.

32. (Cancel) ~~A gate electrode structure as claimed by claim 31 wherein said oxide layer is formed over said N⁺ and P⁺ polysilicon layers.~~

33. (Currently Amended) A gate electrode structure as claimed by claim 31 wherein said oxide layer is formed ~~overon~~ said N⁺ polysilicon layer.

34. (Currently Amended) A gate electrode structure as claimed by claim 31 wherein said oxide layer is formed ~~overon~~ said P⁺ polysilicon layers.

35. (Cancel) ~~A gate electrode structure as claimed by claim 31 wherein said N⁺ polysilicon layer forms a portion of a pull-down transistor and said P⁺ polysilicon layer forms a portion of a pull-up transistor, and said oxide layer is formed over said N⁺ and P⁺ polysilicon layers.~~

36. (Currently Amended) A gate electrode structure as claimed by claim 31 wherein said N⁺ polysilicon layer forms a portion of a pull-down transistor, and said oxide layer is formed ~~overon~~ said N⁺ polysilicon layer.

37. (Currently Amended) A gate electrode structure as claimed by claim 31 wherein said P⁺ polysilicon layer forms a portion of a pull-up transistor, and said oxide layer is formed ~~overon~~ said P⁺ polysilicon layer.

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38. (Previously presented) A gate electrode structure as claimed by claim 31 wherein said oxide layer is silicon dioxide.

39. (Previously presented) A gate electrode structure as claimed by claim 31 wherein said oxide layer has a thickness under 125 Å.

40. (Currently Amended) A memory cell comprising:

- a semiconductor substrate having first and second gate oxide layers;
- a P well formed in said semiconductor substrate;
- a N well formed in said semiconductor substrate adjacent to said P well;
- a N type active region defined in said P well;
- a P type active region defined in said N well;
- an isolation region arranged to isolate said N type active region from said P type active region, and separate said first and second gate oxide layers; and
- a gate electrode structure having a film with an N+ polysilicon layer on said first gate oxide layer over said N type active region and on a first portion of said isolation region, and a P+ polysilicon layer on said second gate oxide layer over said P type active region and on a second portion of said isolation region, an oxide layer formed ~~over~~ on a portion of said film and over only one of said first and second portions of said isolation region, and a metal, metal silicide, or metal nitride film overlaying said film and said oxide layer.